UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,601	10/23/2001	Edward L. Hepler	I-2-183.1US	5329

24374 7590 09/26/2005

VOLPE AND KOENIG, P.C.
DEPT. ICC
UNITED PLAZA, SUITE 1600
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103

EXAMINER	
ABRISHAMKAR, KAVEH	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,601	HEPLER, EDWARD L.	
	Examiner	Art Unit	
	Kaveh Abrishamkar	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is in response to the amendment filed on July 18, 2005. Claims 1-12 were originally received for consideration. Per the received amendment, claims 2,4,6, and 8 are amended, and claims 3,5,7,and 9-12 are cancelled. Claims 1-2,4,6, and 8 are currently being considered.

Response to Arguments

2. Applicant's arguments filed July 18, 2005 have been fully considered but they are not persuasive because:

Regarding independent claims 1,2,4,6 and 8, the applicant argues that the secondary reference, Chan (U.S. Patent No. 6,262,751), does not teach "reordering bits from least significant to most significant." This argument is not found persuasive. As stated in the previous Office action, Chan teaches a system wherein "the top switch circuit 94a in the first switch bank receives bits 7 and 5, where bit 7 is the most-significant bit" (Figure 10, column 7 lines 1-15). Bit 7 is the first bit to be reordered according to Figure 10. Furthermore, Chan discloses that "the output bits can be reordered as to enable the proper data to be selected for a given scan" (column 7 lines 16-20), so the bits can be reordered in any desirable way to enable the proper data for a particular scan. The actual limitation of "reordering bits from least significant to most

significant" was not found in the specification, so the purpose of such an action is ambiguous, therefore, it is believed that the CPA does teach "reordering bits from least significant to most significant." The rejection for the pending claims are maintained as given below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2,4,6, and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Naruse (U.S. Patent 6,115,410) in view of Chan (U.S. Patent 6,262,751).

4. Naruse and Chan are analogous art because both solve the problem of orthogonality in data to be processed.

5. With respect to claim 1, Naruse discloses a system for generating an OVSF code comprising:

A binary counter for providing a binary count comprising a plurality of sequential M-bit binary numbers (column 5 lines 51-56);

An index selector, for providing an M-bit binary identification of said OVSF code (column 5, lines 51-56); and

A logical reduction means having a first input from the counter and a second input from the index selector and having an output; whereby the desired OVSF code is output from said output (column 5 lines 59-67).

6. Naruse does not disclose a system comprising:

Bit reordering means, for selectively reordering the bits of each said binary number from least significant bit to most significant bit.

Chan discloses a system comprising:

Bit reordering means, for selectively reordering the bits of each said binary number from least significant bit to most significant bit (Figure 10).

7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chan with the teachings of Naruse in order to select the proper bits to be used for a given scan (column 7, lines 16-18).

8. With respect to claim 8, Naruse does not disclose a code generator further comprising a switch coupled to said bit reordering means, whereby when the switch is in a first position, the bit reordering means is coupled to the output of said counter to reorder the bits of said binary number, and when the switch is in a second position, the

bit reordering means is decoupled from the output of said counter and the bits of said binary number are not reordered.

Chan discloses a code generator further comprising a switch coupled to said bit reordering means, whereby when the switch is in a first position, the bit reordering means is coupled to the output of said counter to reorder the bits of said binary number, and when the switch is in a second position, the bit reordering means is decoupled from the output of said counter and the bits of said binary number are not reordered (column 6, lines 64-67 through column 7 lines 1-24).

9. It would have been obvious to one of ordinary skill in the art at the time of invention to have combined the teachings of Chan with the teachings of Naruse in order to select the proper bits to be used for a given scan (column 7 lines 16-18).

10. With respect to claim 2, Naruse discloses a code generator for generating individual binary codes of a set of binary codes, each binary codes having 2^M bits, the code generator comprising:

a counter having an output and sequentially outputting M-bit counts in a parallel orientation, each successive count being incremented by 1 (column 5, lines 51-56);

an index selector for outputting an M-bit code identifier in a parallel orientation (column 5 lines 51-56);

a parallel array of M logical gates, each having an output and a first input being one parallel bit from said bit ordering means and a second input being one parallel bit from said index selector (column 5, lines 59-67); and

and a reduction network of logical gates associated with the outputs of said parallel array of logical gates for outputting a single code bit each time a parallel M-bit count is input to said parallel logical gate array from said bit ordering means, such that the binary code which is identified by the M-bit code identifier is produced after 2^M iterations (column 5 lines 59-67).

11. Naruse does not disclose a system comprising:

Bit reordering means, coupled to said output of said counter, for receiving each M-bit count, whereby the M-bit counts are ordered from least significant bit to most significant bit, and whereby said bit reordering means reorders the bits from most significant to least significant bit.

Chan discloses a system comprising:

Bit reordering means, for selectively reordering the bits of each said binary number from least significant bit to most significant bit (Figure 10).

12. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chan with the teachings of Naruse in order to select the proper bits to be used for a given scan (column 7, lines 16-18).

13. With respect to claim 4, Naruse discloses a system for generating a desired pseudorandom code comprising:

a binary counter for providing a plurality of M-bit sequential binary numbers (column 5 lines 51-56);

an index selector, for outputting an M-bit code identifier of the desired pseudorandom code (column 5 lines 51-56);

at least M logical gates, each having a first input from the said bit ordering means and a second input from the index selector, and each having an output (column 5 lines 59-67);

and an XOR tree for XORing said outputs of said logical gates to provide an XORed output; whereby the desired pseudorandom code is output from said XORed output (Figure 4).

14. Naruse does not disclose a system comprising:

Bit reordering means for reordering the bits of said binary counter from least significant bit to most significant bit.

Chan discloses a system comprising:

Bit reordering means for reordering the bits of said binary counter from least significant bit to most significant bit.(Figure 10).

15. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chan with the teachings of Naruse in order to select the proper bits to be used for a given scan (column 7, lines 16-18).

16. With respect to claim 6, Naruse discloses a code generator for generating an individual binary code from a set of N binary codes, each binary code having M bits, the code generator comprising:

a counter having an output and sequentially outputting M-bit binary numbers, each successive binary number being incremented by 1 (column 5 lines 51-56);

an index selector for outputting an M-bit code (column 5 lines 51-56);

a logical gate array having a first input from said bit ordering means and a second input from said index selector, and having an output (column 5 lines 59-67);

a reduction network of logical gates associated with the output of said logical gate array for outputting a single code bit each time an M-bit binary number is input to said logical gate array from said bit reordering means, such that the binary code identified by the M-bit code is produced after 2^M iterations (column 5 lines 59-67).

17. Naruse does not disclose a system comprising:

bit reordering means, coupled to said output of said counter, for receiving each M-bit binary number having bits ordered from least significant bit to most significant bit, whereby said bit reordering means reorders the bits from most significant bit to least significant bit.

Chan discloses a system comprising:

bit reordering means, coupled to said output of said counter, for receiving each M-bit binary number having bits ordered from least significant bit to most significant bit, whereby said bit reordering means reorders the bits from most significant bit to least significant bit.(Figure 10).

18. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chan with the teachings of Naruse in order to select the proper bits to be used for a given scan (column 7, lines 16-18).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaveh Abrishamkar whose telephone number is 571-272-3786. The examiner can normally be reached on Monday thru Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Primary Examiner
AU2131
9/22/05

KA
09/20/2005